

**IN THE CLAIMS:**

Claims 37 through 39 have been amended herein, and new claims 55 through 64 have been added. Claims 52 through 54 have been canceled in response to the restriction requirement.

Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

1-36. (Cancelled).

37. (Currently Amended) A method of preventing a circuit having a test test mode entry function from entering a subsequent test mode after the circuit enters a first test mode, comprising:

initiating a test mode blocking signal after the circuit completes the first test mode; and exclusively controlling the test mode entry function of the circuit with the test mode blocking signal.

38. (Currently Amended) The method of in claim 37, further comprising generating the test mode blocking signal responsive to a final test latch of the circuit during during the first test mode.

39. (Currently Amended) The method of in claim 38, further comprising originating the test mode blocking signal from the circuit.

40-54. (Cancelled).

55. (New) The method of claim 37, further comprising resetting the blocking signal in response to a reception o f a reset prompt signal.

56. (New) The method of claim 37, wherein the initiating a test mode blocking signal is in response to receipt of a test-mode-end signal.

57. (New) The method of claim 37, wherein exclusively controlling with the test blocking signal includes gating the test mode entry function with one of an OR, NOR, AND, or NAND logic gate.

58. (New) The method of claim 37, further comprising preserving a state of an output of the circuit responsive to the test mode entry function in response to activation of the test mode blocking signal.

59. (New) The method of claim 37, wherein the test mode blocking signal is an output of the circuit responsive to the test mode entry function.

60. (New) The method of claim 37, wherein initiating a test mode blocking signal comprises:

initiating a latch mode;  
accepting an input signal;  
performing a logic operation on the input signal;  
deriving an output signal; and  
initiating the test mode blocking signal.

61. (New) The method of claim 60, wherein the deriving an output signal comprises deriving a plurality of output signals, and wherein the test mode blocking signal is one of the plurality of output signals.

62. (New) The method of claim 61, further comprising reestablishing the latch mode through a reset signal.

63. (New) The method of claim 62, further comprising reestablishing the latch mode exclusively through the reset signal.

64. (New) The method in claim 63, wherein reestablishing the latch mode through the reset signal comprises resetting the one of the plurality of output signals that initiated the input lockout mode.